RECEIVED
CENTRAL FAX CENTER
JUL 20 2007

Remarks/Arguments

Claims 1, 2 and 4-20 are pending in this application, and are rejected in the final Office Action of April 30, 2007. Claims 1, 10, 14 and 15 are amended herein to more particularly point out and distinctly claim the subject matter Applicant regards as the invention.

Re: Rejection of Claims 1-4 and 14-15

Claims 1-2 and 4-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of U.S. Patent No. 5,606,443 issued to Sgambati (hereinafter, "Sgambati"). Applicant respectfully traverses this rejection for at least the following reasons.

It is first noted that independent claims 1 and 15, as amended herein, recite:

> "a control circuit for inhibiting the signals transmitted from the output line of the second circuit to the input line of the first circuit when the first circuit is transmitting signals to the input line of the second circuit and thereby preventing the first circuit from generating an interrupt signal" (emphasis added; see claim 1), and

> "if the mode is a second mode, detecting whether the receiver-transmitter circuit is transmitting signals to the serial interface circuit, and if the receiver-transmitter circuit is transmitting signals to the serial interface circuit, prohibiting the serial interface circuit from transmitting signals to the receiver-transmitter circuit and thereby preventing the receiver-transmitter circuit from generating an interrupt signal" (emphasis added; see claim 15)

As indicated above, independent claims 1 and 15 are amended herein to clarify that inhibiting the signals transmitted from the output line of the second circuit (the serial interface circuit in claim 15) to the input line of the first circuit (the receiver-transmitter circuit in claim 15) when the first circuit is transmitting signals to the input line of the second circuit prevents the first circuit from generating an interrupt signal. Preventing the generation of an unnecessary interrupt signal by the first circuit in this manner solves the specific problem addressed on page 2 of Applicant's disclosure.

Neither Applicant's admitted prior art nor Sgambati, whether taken individually or in combination, teach or suggest, *inter alia*, the aforementioned feature of independent claims 1 and 15. In particular, Applicant's admitted prior art shown in FIG. 1 of Applicant's disclosure fails to teach or suggest any means for inhibiting the signals transmitted from the output line of G-LINK circuit 10 to the input line of UART 12 when UART 12 is transmitting signals to the input line of G-LINK circuit 10 and thereby fails to prevent UART 12 from generating an unnecessary interrupt signal. Sgambati is unable to remedy this deficiency of Applicant's admitted prior art. In particular, Sgambati discloses a circuit for inhibiting the passage of signals through a particular circuit element (e.g., NOR gate 140 – see column 6, lines 28-35). However, like Applicant's admitted prior art, Sgambati also fails to teach or suggest inhibiting signal transmission to thereby prevent a given circuit from generating an interrupt signal, as claimed. Accordingly, neither Applicant's admitted prior art nor Sgambati recognize or address the specific problem that is solved by the inventions of independent claims 1 and 15. Therefore, independent claims 1 and 15 and their respective dependent claims are deemed allowable over the proposed combination of Applicant's admitted prior art and Sgambati, and withdrawal of the rejection is respectfully requested.

Re: Rejection of Claims 1 and 15

Claims 1 and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of Korean Patent document 20010661358 to Park (hereinafter, "Park"). Applicant respectfully traverses this rejection for at least the following reasons.

As indicated above, independent claims 1 and 15 are amended herein to clarify that inhibiting the signals transmitted from the output line of the second circuit (the serial interface circuit in claim 15) to the input line of the first circuit (the receiver-transmitter circuit in claim 15) when the first circuit is transmitting signals to the input line of the second circuit prevents the first circuit from generating an interrupt signal.

Neither Applicant's admitted prior art nor Park, whether taken individually or in combination, teach or suggest, *inter alia*, the aforementioned feature of independent

claims 1 and 15. As indicated above, Applicant's admitted prior art shown in FIG. 1 of Applicant's disclosure fails to teach or suggest any means for inhibiting the signals transmitted from the output line of G-LINK circuit 10 to the input line of UART 12 when UART 12 is transmitting signals to the input line of G-LINK circuit 10 and thereby fails to prevent UART 12 from generating an unnecessary interrupt signal. Park is unable to remedy this deficiency of Applicant's admitted prior art. In particular, Park discloses a half-duplex communication control circuit which blocks reception data in the case of transmission and prevents transmission data in the case of reception (see Abstract). However, like Applicant's admitted prior art, Park also fails to teach or suggest inhibiting signal transmission to thereby prevent a given circuit from generating an interrupt signal, as claimed. Accordingly, neither Applicant's admitted prior art nor Park recognize or address the specific problem that is solved by the inventions of independent claims 1 and 15. Therefore, independent claims 1 and 15 and their respective dependent claims are deemed allowable over the proposed combination of Applicant's admitted prior art and Park, and withdrawal of the rejection is respectfully requested.

Re: Rejection of Claims 1 and 15

Claims 1 and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of U.S. Patent No. 6,367,079 issued to DeVos et al. (hereinafter, "DeVos"). Applicant respectfully traverses this rejection for at least the following reasons.

As indicated above, independent claims 1 and 15 are amended herein to clarify that inhibiting the signals transmitted from the output line of the second circuit (the serial interface circuit in claim 15) to the input line of the first circuit (the receiver-transmitter circuit in claim 15) when the first circuit is transmitting signals to the input line of the second circuit prevents the first circuit from generating an interrupt signal.

Neither Applicant's admitted prior art nor DeVos, whether taken individually or in combination, teach or suggest, *inter alia*, the aforementioned feature of independent claims 1 and 15. As indicated above, Applicant's admitted prior art shown in FIG. 1 of

Applicant's disclosure fails to teach or suggest any means for inhibiting the signals transmitted from the output line of G-LINK circuit 10 to the input line of UART 12 when UART 12 is transmitting signals to the input line of G-LINK circuit 10 and thereby fails to prevent UART 12 from generating an unnecessary interrupt signal. DeVos is unable to remedy this deficiency of Applicant's admitted prior art. In particular, DeVos discloses a control circuit 22 for controlling signal transmission between an ATM interface circuit 29 and a physical storage medium 21 (see FIG. 2A). However, like Applicant's admitted prior art, DeVos also fails to teach or suggest inhibiting signal transmission to thereby prevent a given circuit from generating an interrupt signal, as claimed. Accordingly, neither Applicant's admitted prior art nor DeVos recognize or address the specific problem that is solved by the inventions of independent claims 1 and 15. Therefore, independent claims 1 and 15 and their respective dependent claims are deemed allowable over the proposed combination of Applicant's admitted prior art and DeVos, and withdrawal of the rejection is respectfully requested.

Conclusion

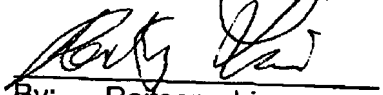
Having fully addressed the Examiner's rejections it is believed that, in view of the accompanying amendments and remarks/arguments, this application stands in condition for allowance. Accordingly, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6813, so that a mutually convenient date and time for a telephonic interview may be scheduled. No fee is believed due. However, if a fee is due, please charge the fee to Deposit Account 07-0832.

Applicant's disclosure fails to teach or suggest any means for inhibiting the signals transmitted from the output line of G-LINK circuit 10 to the input line of UART 12 when UART 12 is transmitting signals to the input line of G-LINK circuit 10 and thereby fails to prevent UART 12 from generating an unnecessary interrupt signal. DeVos is unable to remedy this deficiency of Applicant's admitted prior art. In particular, DeVos discloses a control circuit 22 for controlling signal transmission between an ATM interface circuit 29 and a physical storage medium 21 (see FIG. 2A). However, like Applicant's admitted prior art, DeVos also fails to teach or suggest inhibiting signal transmission to thereby prevent a given circuit from generating an interrupt signal, as claimed. Accordingly, neither Applicant's admitted prior art nor DeVos recognize or address the specific problem that is solved by the inventions of independent claims 1 and 15. Therefore, independent claims 1 and 15 and their respective dependent claims are deemed allowable over the proposed combination of Applicant's admitted prior art and DeVos, and withdrawal of the rejection is respectfully requested.

Conclusion

Having fully addressed the Examiner's rejections it is believed that, in view of the accompanying amendments and remarks/arguments, this application stands in condition for allowance. Accordingly, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6813, so that a mutually convenient date and time for a telephonic interview may be scheduled. No fee is believed due. However, if a fee is due, please charge the fee to Deposit Account 07-0832.

Respectfully submitted,



By: Reitseng Lin
Reg. No. 42,804
Phone (609) 734-6813

Patent Operations
Thomson Licensing L.L.C.
P.O. Box 5312
Princeton, New Jersey 08540